

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)	
)	
Fouad A. Faour et al.)	
)	Group Art Unit: 2859
Serial No.: 10/817,265)	
)	Examiner: Verbitsky, Gail Kaplan
Filed: April 2, 2004)	
)	Atty. Docket: 10030219-1
For: TEMPERATURE)	
MEASUREMENT OF AN)	
INTEGRATED CIRCUIT)	
)	

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop: Amendment

Dear Sir:

In response to the Final Office Action mailed on April 5, 2007 the applicants appeal as follows:

This brief contains items under the following headings as required by 37 CFR §41.37 and MPEP §1206:

- I. Real Party In Interest
- II. Related Appeals, Interferences and Judicial Proceedings
- III. Status of Claims
- IV. Status of Amendments
- V. Summary of Claimed Subject Matter
- VI. Grounds of Rejection to be Reviewed on Appeal
- VII. Argument
- VIII. Claims
- IX. Evidence
- X. Related Proceedings

Appendix A	Claims
Appendix B	Evidence
Appendix C	Related Proceedings

(I) REAL PARTY IN INTEREST

The real party in interest is AVAGO GENERAL IP (SINGAPORE) PTE. LTD., a Singapore corporation. .

(II) RELATED APPEALS, INTERFERENCES AND JUDICIAL PROCEEDINGS

There are no related appeals, interferences or judicial proceedings currently known to the Appellants, Appellants' legal representatives or the assignee, which will directly affect, or be directly affected by, or have a bearing on, the Board's decision.

(III) STATUS OF CLAIMS

Claims 1-4 and 7-19 are pending and rejected. The rejections of claims 1-4 and 7-19 are appealed.

(IV) STATUS OF AMENDMENTS

No amendments were filed or entered subsequent to the final rejection mailed April 5, 2007.

(V) SUMMARY OF THE CLAIMED SUBJECT MATTER

The invention as claimed is summarized below with reference numerals and references to the specification and drawings. The invention is broadly set forth in the language corresponding to independent claim 1. Discussions about elements of the invention can be found at least in the locations in the specification and drawings cited in the claim below.

CLAIM 1

An integrated circuit (200), comprising:
a number of pads (202, 204, 206) [Figs 2 and 4; Paragraphs 18 and 27];
a constant current source (208) to provide a current (I) [Fig. 2; Paragraphs 18 and 19];
a thermal diode (210) that receives said current (I), said thermal diode (210) being coupled between first and second ones (202, 204) of said pads (202, 204, 206) [Fig. 2; Paragraphs 18 and 19]; and
an analog to digital converter (216) to i) receive a forward bias voltage (v) of the thermal diode (210), and ii) output a digital representation of the forward bias voltage (v) [Fig. 2; Paragraphs 20 and 21];
wherein a third one (206) of said pads (202, 204, 206) is provided to receive a reference current, said third pad being (206) coupled to an input of said constant current source (208), said reference current serving to control the constant current source (208) [Fig. 2; Paragraph 18].

CLAIM 7

An integrated circuit (400), comprising:
a constant current source (402) to provide first and second currents (I_1 , I_2) of different magnitudes [Fig. 4; Paragraphs 26];
first and second thermal diodes (404, 406) that respectively receive said first and second currents (I_1 , I_2) [Fig. 4; Paragraph 26];
a comparator (408) to receive forward bias voltages (v_1 , v_2) of each of the thermal diodes (404, 406), to compare the forward bias voltages (v_1 , v_2), and to output a voltage difference indicative of a temperature of the integrated circuit (400) [Fig. 4; Paragraphs 26 and 28]; and

a pad (410) to receive a reference current (I_{ref}), said pad (410) being coupled to an input of said constant current source, said reference current (I_{ref}) serving to control the constant current source (402) [Fig. 4; Paragraph 27].

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 and 7-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) in view of Deng (6,911,861).

Claims 4 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) and prior art as applied to claims 1-3 and 7-17, and further in view of Vergis (U.S. 6,453,218).

Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) and prior art as applied to claims 1-3 and 7-17, and further in view of Audy (5,195,827).

The appellants contend that the rejections are in error.

(VII) ARGUMENT

I. Rejection of Claims 1-3, and 7-17 Under 35 U.S.C. §103(a)

Claims 1-3, and 7-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) in view of Deng (U.S. 6,911,861).

CLAIM 1

Claim 1 reads as follows:

An integrated circuit, comprising:
a number of pads;
a constant current source to provide a current;
a thermal diode that receives said current, said thermal diode being coupled between first and second ones of said pads; and
an analog to digital converter to i) receive a forward bias voltage of the thermal diode, and ii) output a digital representation of the forward bias voltage;
wherein a third one of said pads is provided to receive a reference current, said third pad being coupled to an input of said constant current source, said reference current serving to control the constant current source.

Some portions of claim 1 that are not disclosed by either Davidson or Deng, or their combination, have been printed above in bold type.

According to the final office action, Davidson discloses a constant current source in Fig. 2, wherein the current supplied by the constant current source is referred to as I_1 . The applicants note that the current I_1 is simply the current that passes through a

resistor R_1 and that it is not constant; nor can the current be constant. Rather, per Ohm's law, the current I_1 is proportional to the resistances, R_1 , R_3 , R_0 , and the resistance of components connected to the output $C4_A$. In addition, the current I_1 is also proportional to the forward voltage of the OCT diode D_1 . However, the forward voltage of OCT diode D_1 changes with temperature and is measured in order to measure the temperature of the diode D_1 . As the forward voltage changes, the current I_1 will change. Thus, the voltage supply V_P cannot supply a constant current as claimed in claim 1. In order for the current I_1 to be constant, the forward voltage of diode D_1 would have to be constant, which is inconsistent with using the forward voltage of diode D_1 to measure temperature; the forward voltage is a function of temperature.

Based on the foregoing, the references, taken individually or in combination, do not disclose the constant current source of claim 1 and, therefore, they cannot render claim 1 obvious.

The final office action states that Davidson does not teach "wherein a third one of said pads is provided to receive a reference current, said third pad being coupled to an input of said constant current source, said reference current serving to control the constant current source" as claimed in claim 1. The final office action tries to rely on Fig. 1 of Deng (prior art) to show this element of claim 1. According to the final office action, a current generating circuit 104 generates a current proportional to a reference current being regulated (controlled/adjusted) by a resistor coupled to the circuit by means of a third pad 108. According to the final office action, the prior art discloses a variable current reference, which is used to adjust the constant current source.

The prior art circuit disclosed in Deng is related to a current source, wherein the output current is controlled by a voltage V_{BG} , not an input current received on a third pad as claimed. Accordingly, Deng receives a reference voltage and outputs a current based on the voltage. Claim 1, on the other hand, recites receiving a reference current, not a reference voltage, and outputting a constant current based on the reference current. Thus, neither Davidson, Deng, nor their combination, disclose all the elements of claim 1 and cannot render claim 1 obvious.

In addition to the foregoing, the applicants contend that Deng does not disclose, “wherein a third one of said pads is provided to receive a reference current, said third pad being coupled to an input of said constant current source, said reference current serving to control the constant current source” as claimed in claim 1. The applicants further contend that such a combination with Davidson would not work and is therefore improper.

With regard to the third pad, the final office action states that C4_B of Davidson constitutes the claimed third pad, wherein the third pad is provided to receive a reference current. Per the schematic diagram of Fig. 1, pad C4_B is designed to receive the current that drives the OCT diode D₁ and is not provided to receive a reference current that serves to control a constant current source as claimed in claim 1. Thus, the final office action has failed to disclose the claimed third pad.

In addition to the foregoing, there is no description provided in the final office action as to how the prior art circuit of Deng can be added to the circuit of Davison so that Davidson could receive the reference current and the reference current could serve to control a constant current source of Davidson. As stated above, Davidson does not even disclose a constant current source. According to MPEP §706.02(j)(C), the Examiner should set forth the proposed modification of the applied references necessary to arrive at the claimed subject matter. The description in the final office action does not provide any explanation as to how these references can be combined in order to render claim 1 obvious. For example, there is no description as to how a reference current could be received on pad C4_B of Davidson so as to control a constant current source. This proposed circuit simply would not work.

Based on the foregoing, the applicants contend that the rejection under 35 U.S.C. §103(a) has been overcome and the applicants request that rejection of claim 1 be overturned.

CLAIMS 2 AND 3

Claims 2 and 3 are dependent on claim 1 and will stand or fall with claim 1 solely for the purposes of this appeal.

CLAIM 7

Claim 7 reads as follows:

An integrated circuit, comprising:
a constant current source to provide first and second currents of different magnitudes;
first and second thermal diodes that respectively receive said first and second currents;
a comparator to receive forward bias voltages of each of the thermal diodes, to compare the forward bias voltages, and to output a voltage difference indicative of a temperature of the integrated circuit; and
a pad to receive a reference current, said pad being coupled to an input of said constant current source, said reference current serving to control the constant current source.

Some portions of claim 7 that are not disclosed by either Davidson or Deng, or their combination, have been printed above in bold type.

Claim 7 was rejected based on many of the same grounds as the rejection of claim 1. Accordingly, the applicants incorporate the rebuttal to the rejection of claim 1 into this rebuttal of the rejection of claim 7.

As stated above, Davidson does not disclose a constant current source as claimed in claim 7. Rather, Davidson discloses a power supply, that outputs current, which is not necessarily constant. Thus, there is no constant current source disclosed

in Davidson as stated in the final office action. In addition, there is no third pad disclosed in Davidson. As stated above, the pad $C4_B$ receives the current to drive an OCT diode and it does not receive a reference current as stated in the final office action. Even if pad $C4_B$ received a reference current, there is no way that a current received on pad $C4_B$ can control a constant current source as claimed in claim 7.

As also stated above, Deng discloses a current source that is regulated by an input voltage, not a reference current as claimed in claim 7. More specifically and as stated above, Deng discloses a voltage V_{BG} that controls a reference current. Claim 7, on the other hand, recites a reference current used to control a constant current source. Therefore, the references, taken individually or in combination, do not disclose all the elements of claim 7 and cannot render claim 7 obvious.

Based on the foregoing, the rejection of claim 7 has been overcome and the applicants respectfully request that the rejection be reversed.

CLAIMS 8-17

Claims 8-17 are dependent on claim 7 and will stand or fall with claim 7 solely for the purposes of this appeal. Accordingly, the applicants request that the rejections be reversed.

II. Rejection of Claims 4 and 19 Under 35 U.S.C. §103(a)

Claims 4 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) and Deng (U.S. 6,911,861) in view of Vergis (U.S. 6,453,218).

Claims 4 and 19 are dependent on claims 1 and 7, respectively, and will stand or fall with claims 1 and 7 respectively solely for the purposes of this appeal.

III. Rejection of Claim 18 Under 35 U.S.C. §103(a)

Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Davidson (U.S. 5,639,163) and Deng (U.S. 6,911,861) in view of Audy (U.S. 5,195,827).

Claim 18 is dependent on claim 7 and will stand or fall with claim 7 solely for the purposes of this appeal.

In view of the above, all of the pending claims are now believed to be in condition for allowance and a notice to that effect is earnestly solicited.

Respectfully submitted,
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APPENDIX A - CLAIMS

Claim 1 (previously presented): An integrated circuit, comprising:

a number of pads;

a constant current source to provide a current;

a thermal diode that receives said current, said thermal diode being coupled between first and second ones of said pads; and

an analog to digital converter to i) receive a forward bias voltage of the thermal diode, and ii) output a digital representation of the forward bias voltage;

wherein a third one of said pads is provided to receive a reference current, said third pad being coupled to an input of said constant current source, said reference current serving to control the constant current source.

Claim 2 (original): The integrated circuit of claim 1, further comprising logic to receive the digital representation of the forward bias voltage and calculate a temperature of the integrated circuit.

Claim 3 (original): The integrated circuit of claim 2, wherein said logic comprises a temperature look-up table.

Claim 4 (original): The integrated circuit of claim 1, further comprising a register to store the digital representation of the forward bias voltage, said register being readable during normal operation of the integrated circuit.

Claims 5 and 6 (cancelled)

Claim 7 (previously presented): An integrated circuit, comprising:

a constant current source to provide first and second currents of different magnitudes;

first and second thermal diodes that respectively receive said first and second currents;

a comparator to receive forward bias voltages of each of the thermal diodes, to compare the forward bias voltages, and to output a voltage difference indicative of a temperature of the integrated circuit; and

a pad to receive a reference current, said pad being coupled to an input of said constant current source, said reference current serving to control the constant current source.

Claim 8 (original): The integrated circuit of claim 7, wherein the thermal diodes are positioned adjacent one another.

Claim 9 (original): The integrated circuit of claim 7, wherein the first and second currents have a known relationship.

Claim 10 (original): The integrated circuit of claim 7, wherein the second current is an integer multiple of the first current.

Claim 11 (original): The integrated circuit of claim 7, wherein the comparator is a differential amplifier.

Claim 12 (original): The integrated circuit of claim 11, further comprising an analog to digital converter to i) receive the voltage difference output by the differential amplifier, and ii) output a digital representation of the voltage difference.

Claim 13 (original): The integrated circuit of claim 12, further comprising logic to receive the digital representation of the voltage difference and calculate a temperature of the integrated circuit.

Claim 14 (original): The integrated circuit of claim 7, further comprising an analog to digital converter to i) receive the voltage difference output by the comparator, and ii) output a digital representation of the voltage difference.

Claim 15 (original): The integrated circuit of claim 14, further comprising logic to receive the digital representation of the voltage difference and calculate a temperature of the integrated circuit.

Claim 16 (original): The integrated circuit of claim 15, wherein said logic is configured in accordance with a known relationship between the first and second currents.

Claim 17 (original): The integrated circuit of claim 15, wherein said logic comprises a temperature look-up table.

Claim 18 (original): The integrated circuit of claim 15, further comprising one or more analog to digital converters to i) respectively receive said first and second currents, and ii) output digital representations of said first and second currents to said logic.

Claim 19 (original): The integrated circuit of claim 14, further comprising a register to store the digital representation of the voltage difference, said register being readable during normal operation of the integrated circuit.

Claim 20 (cancelled)

APPENDIX B - EVIDENCE

There is no evidence to be presented

APPENDIX C - RELATED PROCEEDINGS

There are no related proceedings.